

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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	§	
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	§	
Serial No.: 10/695,408	§	Confirmation No. 5639
	§	
Filed: October 28, 2003	§	Examiner: Scott C. Sun
	§	
For: APPARATUS AND METHOD FOR	§	
DATA MIGRATION IN A STORAGE	§	Docket No. 112-0122US
PROCESSING DEVICE	§	

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**REPLY BRIEF**

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**I. STATUS OF CLAIMS**

Claims 1-36 are rejected. The appealed claims are 1-36.

**II. GROUND OF REJECTION TO BE REVIEWED ON APPEAL**

Claims 1-36 stand rejected under 35 U.S.C. § 102 over Testardi, U.S. Patent Appln. 2003/0140210. Applicants thank the Examiner for indicating the withdrawal of the § 112, ¶ 2 rejections.

**III. ARGUMENT**

The following arguments are in rebuttal to the Examiner's Answer mailed April 30, 2008 and are supplementary to the originally-filed appeal brief. Appellants maintain the positions set forth in that brief in their entirety. Accordingly, failure to address grounds of rejection in this reply brief should not be construed as acquiescence by Appellants to the Examiner's position.

**A. Section 102 Rejections**

**1. Claims 19, 1, 10 and 28**

The Answer quotes ¶ 62, a general, high level description of the data storage system 12 including a switching fabric 20 done in conjunction with Fig. 3, which is stated as being a logical view of one embodiment. Applicants acknowledge that the switching fabric 20 may include one or more switches. But the high level, general statement made in ¶ 62 must also be considered in light of the more specific teachings of Figs. 4B and 4C, which provide details as to the switches. Fig. 4B shows one switch with directly attached hosts and storage units. As the hosts and storage units are not part of the switching fabric 20, Fig. 4B conforms to the teachings of ¶ 62. Fig. 4C shows these switches, thus clearly conforming to the teachings of ¶ 62, but as Applicants have noted, only hosts have been connected to the new switches. The discussion of Fig. 4C at ¶ 79 clearly indicates that the FPs are only in switch 43, not in switches 47a, 47b, the switches added to Fig. 4B to form Fig. 4C. Thus the FPs, the element corresponded to the claimed I/O module, are only in the switch 43. As the rejection has indicated the CP, which was

corresponded to the claimed control module, is illustrated in Figs. 4A, 4B, and 4C, it must also reside in the switch 43 as that is the only common element. Therefore, according to the specific teachings of Testardi, the device corresponded to the claimed storage processing device is the switch 43. As Applicants have argued, Figs. 4B and 4C show the storage units directly connected to the switch 43. Thus, the specific explanation of Testardi teaches that the storage units must be directly connected to the storage processing device. The hosts may be remote through a switch but the storage units must be directly connected. This does not contradict the general statement of ¶ 62, as one or more switches do form the switching fabric, as in Figs. 4B and 4C. The specific teachings provide a different limitation which the general statement of ¶ 62 is not sufficient to overcome.

**2. Claim 3, 12, 17, 21, 26, 30, and 35**

Applicants argued that the operation of the fast path transferring the specified case to the control path, which then forces a retry, does not meet the positive requirement in the claims that the processor perform the delaying operation. The Answer argues that the fast path is at least partially responsible for the delaying because the decision to pass the operation is performed by the fast path. Carrying the logic of the Answer to the next step would lead to the host itself also delaying the operation because it sent the write request which is to be delayed. Without that write request there would be nothing to delay, thus the host is also at least partly responsible for delaying the operation. Taking it to an even more extreme level, a user would also be partly responsible for delaying the operation because the user had the host perform the operation which resulted in the write request. Yet no one would reasonably argue that the host or the user are delaying the write operation, yet they meet the logic used by the Answer. These examples have been used to illustrate the error in the logic used in the Answer. As Applicants have stated, the fast path simply passes off the operation to the continual path. This does not meet the positive claim requirement of the processors delaying the write operation.

**B. Conclusion**

For the reasons stated above, and set forth in the originally-filed appeal brief, Applicants respectfully submit that the rejections should be reversed. Additionally, to the extent specific

claims have not been addressed, these claims depend from one or more claims that have been specifically addressed, and are therefore patentable for at least the same reasons as the claims specifically addressed. Applicants further believe that they have complied with each requirement for an appeal brief and for a reply brief.

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the prior art which have yet to be raised, but which may be raised in the future.

If any fees are required or have been overpaid, please appropriately charge or credit those fees to Deposit Account Number 501922, referencing docket number 112-0122US.

Respectfully submitted,

June 19, 2008

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